REMARKS

The Examiner's Office Action dated on November 3, 2004 has been received and its contents carefully considered.

In this Amendment, the specification has been amended to correct typographical errors noted by Applicants during review of the application. In addition, claims 1, 9, 11, and 16 have been amended. Claims 1, 9, and 16 are the independent claims. Claims 1-22 are now pending in the application. It is submitted that the originally filed application including the specification and drawings support the Amendment and thus no new matter is added therein. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

Claims 1-7, 9-14, and 16-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Kalkunte* in view of *Yoshida*. Claims 1, 9, 11, 16 have been amended to make features of these claims that are inherently patentable over the cited combination more easily understood. Applicants respectfully submit that these claims are patentable over the cited combination for the following reasons.

Regarding claim 1, the Examiner alleges that *Kalkunte*, the primary reference, discloses a transmit process in Figure 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch), and acknowledges that the reference does not teach "a receive process" and "QLNs that hold information corresponding to each packet" that are recited in claim 1 (pages 2-3 of the Office Action). The Examiner, however, alleges that *Yoshida*, the secondary reference, discloses a receive process in column 6, lines 61-64. Moreover, the Examiner alleges that it would have been obvious to one skilled in the art at the time of the invention to use the receive process of *Yoshida* in

conjunction with the transmit process of *Kalkunte*, and that the motivation to do so would be to obtain an optimum transmission time for each packet. With respect to the absence from *Kalkunte* of "QLNs that hold information corresponding to each packet", the Examiner asserts that Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. Further, the Examiner states that it would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN, and that the motivation to do so would be to have all the information for each packet. Applicants respectfully traverse this rejection.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features of the claim.

Applicants' independent claim 1, as amended, is directed to a method for compensating for a clock signal difference between a switch and a peripheral device, the switch being used for receiving and transmitting a plurality of packets, wherein each of the packets corresponds to a queue link node, an N-th packet corresponds to an N-th queue link node QLN(N) and an M-th packet corresponds to an M-th queue link node QLN(M), where N and M are integers. The method recited in claim 1 comprises a receiving process and a transmitting process. According to the **receiving process** of claim 1, when **an (N+1)-th packet is received by the switch, an inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet is recorded into the (N+1)-th queue link node QLN(N+1) corresponding to the (N+1)-th packet**, as recited in steps (a) to (e) of claim 1. According to the **transmitting process** of claim 1, when **the M-th packet is transmitted**

by the switch, the **M-th queue link node QLN(M) is read** for obtaining an **inter-packet gap IPG(M-1, M)**, which is recorded in the M-th queue link node QLN(M) when the M-th packet is received by the switch after the receiving of the (M-1)-th packet, as recited in steps (a1) of claim 1. According to the **transmitting process** of claim 1, after the M-th packet is transmitted by the switch, an (M+1)-th packet is then transmitted after a delay time corresponding to a counted value by a counter, where the counted value is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), as recited in steps (a1) to (e1) of claim 1. That is, when the M-th and (M+1)-th packets are transmitted respectfully, **an inter-packet gap between the transmitted M-th and (M+1)-th packet**s is based on the **inter-packet gap IPG(M-1, M)**, which is the **inter-packet gap between the received (M-1)-th and M-th packets**, and is recorded into the M-th QLN(M) by the receiving process, as performed by steps (a1) to (e1). According to the transmitting and receiving processes of the switch, as recited in claim 1, congestion of the memory of the switch is reduced.

The Examiner alleges that *Kalkunte* discloses a transmit process in FIG. 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch). However, Kalkunte discloses that **each network station 44 controls its transmission of data packets** by implementing an interpacket gap (IPG) delay on a packet-by-packet basis to ensure that its effective data packet transmission rate is in accordance with the desired transmission rate negotiated with the **hub 46** (column 6, lines 27-32). The **hub 46** is implemented as a full-duplex **switch** that simultaneously sends and receives data packets to each of the network stations 44 (column 5, lines 19-21). Moreover, the *Kalkunte* teaches in accordance with FIG. 3A that:

> The method begins in step 60 by station A receiving the desired transmission rate (r_a) from the network manager, illustrated in FIG. 2 as the hub 46. Hence, the network stations A, B, C, D, E44, each receive their respective desired transmission rates r_a, r_b, r_c, r_d, r_e. The desired transmission rate (r_a) is preferably in the form of a time to transmit a bit or byte of data (sec/byte).
>
> **Station A then transmits a first data packet (P1) onto the network in step 62** according to full-duplex Ethernet protocol. **Station A then determines a first delay time (D1) based upon the desired transmission rate (r_a) and the size of the first data packet (P1), described below, and in step 64 waits the determined first delay time (D1) before transmitting a second data packet (P2) step 66.** As described below, the duration of the delay time is directly proportional to the size of the transmitted data packet. Hence, if the transmitted data packet (P1) has a large size, i.e., a large number of bytes, the delay time (D1) has a longer duration to maintain an overall constant output transmission rate.
>
> After transmitting the second packet (P2) in step 66, station A determines a second delay time (D2) based on the size of the second data packet (P2) and the desired transmission rate (r_a), and then waits the second delay time (D2) in step 68. After transmitting the third data packet (D3) in step 70, station A determines a third delay time (D3) based upon the size of the third data packet (P3) and the desired transmission rate (r_a) and then waits the third delay time (D3) in step 72. Hence, the delay between data packet transmissions is determined on a per-packet basis to ensure that the effective transmission rate corresponds to the desired transmission rate. (column 6, lines 33-64) (*emphasis added*)

Kalkunte in the above cited passages teaches a transmit process in order for a **network station** to modify the **inter-packet gaps** between transmitting packets **based on the desired transmission rate (r_a)** negotiated with the **hub 46, which is implemented as a switch, and the size of the data packet to be transmitted.** Thus, it is respectfully submitted that these passages **do not** teach a transmit process for compensating for clock signal difference between switch and peripheral device, as recited in claim 1. In contrast to *Kalkunte*, claim 1 recites the features of recording the inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet into the (N+1)-th queue link node QLN(N+1) when the (N+1)-th packet is received by the switch, as recited in the receiving process of claim 1. In addition, where the inter-packet gap IPG(M-1, M) between the (M-

1)-th packet and the M-th packet is recorded in the M-th queue link node QLN(M) on the receiving of the M-th packet in the receiving process of claim 1, claim 1 recites the features of: reading the M-th queue link node QLN(M) for obtaining the inter-packet gap IPG(M-1, M) when an M-th packet is transmitted by the switch; and basing the inter-packet gap between the transmitted M-th and (M+1)-th packets on the inter-packet gap IPG(M-1, M), as recited in the transmitting process of claim 1. These features of reading the M-th queue link node on receiving the M-th packet and basing the inter-packet gap between the transmitted M-th and (M+1)-th packets on the inter-packet gap IPG(M-1,M) **contrast** with the disclosure of *Kalkute* that a **network station** modifies the **inter-packet gaps** between transmitting packets **based on the desired transmission rate (r_a)** negotiated with the **hub 46, which is implemented as a switch, and the size of the data packet to be transmitted.**

Further, Applicants respectfully submit that the features that are missing from *Kalkunte*, as above discussed, also are missing from *Yoshida*. As acknowledged by the Examiner, a receive process in column 6, lines 61-64 of *Yoshida* is disclosed by the following passage:

> Specifically, whenever a cell is received, the cell interval which is the difference between the time the current cell is received and the time the previous cell was received is calculated, and the count in the leaky bucket counter is decremented by the cell interval value calculated and then supplemented with a given value.

The passage does not teach, disclose, or suggest the features missing from *Kalkunte* as above discussed.

With respect to rejection of claim 1, the Examiner admits "QLNs that hold information corresponding to each packet" are missing from *Kalkunte*. However, the Examiner alleges that:

> Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.

Applicants respectfully disagree with this assertion.

As set forth in MPEP §2143, when applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:

> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.
>
> *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

In addition, according to MPEP §2143.03, "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Thus, only considering queue link nodes *separately*, the broad assertions: "Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet"; "It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN""; and

"The motivation would be to have all the information for each packet," are insufficient to support a conclusion that queue link nodes and the features related to the queue link nodes corresponding to inter-packet gaps, as recited in claim 1, would obvious to one of ordinary skill in the art at the time of the invention was made.

As above mentioned, claim 1 teaches that the inter-packet gap IPG(M-1, M) between the (M-1)-th packet and the M-th packet is recorded into the M-th queue link node QLN(M) on the receiving of the M-th packet in the receiving process, and the inter-packet gap IPG(M-1, M) is read from the QLN(M) and utilized as the basis of the inter-packet gap between the transmission of the M-th and (M+1)-th packets in the transmitting process. It is therefore respectfully submitted that the assertion of motivation to combine and modify at issue does not consider all the features of claim 1 ***as a whole***. In view of the role of queue link nodes and the related features of claim 1 corresponding to inter-packet gaps in both the receiving and transmitting processes recited in claim 1, Applicants respectfully submit that the cited combination fails to teach, disclose, or suggest all features relating to queue link nodes corresponding to packets, as recited in claim 1.

As shown above, the features regarding queue link nodes in the transmitting and receiving processes of claim 1 are missing from both *Kalkunte* and *Yoshida*. In particular, the cited combination fails to disclose, teach, or suggest the features, among others, that: when the M-th and (M+1)-th packets are transmitted respectfully, **a inter-packet gap between the transmitted M-th and (M+1)-th packet**s is based on the **inter-packet gap IPG(M-1, M)**, which is the **inter-packet gap between the received (M-1)-th and M-th packets** and is recorded into the M-th QLN(M) by the receiving process, as performed by steps (a1) to (e1) of the transmitting process of claim 1. Applicants respectfully assert that

no teaching, suggestion, or motivation is provided in the Office Action to motivate one of ordinary skill at the time of the invention was made to modify the prior art references to meet all features of claim 1. Thus, the combination of teachings from *Kalkunte* with *Yoshida* in the manner suggested by the Examiner does not disclose, teach, or even suggest all features of claim 1. For at least these reasons, it is respectfully submitted that claim 1 is patentable over *Kalkunte* in view of *Yoshida*, and the rejection of claim 1 accordingly should be withdrawn.

Moreover, it is respectfully submitted that the rejection of claims 2-7 should be withdrawn, and the claims should be allowed, for at least the reason that they depend from independent claim 1 as well as for the additional features therein.

Regarding Applicants' independent claim 9, it is noted that the reasons presented for rejecting claim 9 are based on those presented for rejecting claim 1. Where the recitation of (1) the switch comprising a receive media access control (RMAC) unit for receiving a plurality of packets, a transmit media access control (TMAC) unit for receiving the packets, a first counter and a second counter; and (2) queue link nodes corresponding to packets with inter-packet gaps are missing from a proposed combination of the receive process of *Yoshida* with the transmit process of *Kalkunte*, as provided from page 3, line 11 to page 4, line 3 of the reasons for rejecting claim 7, the Examiner further alleges (on page 4) that:

> A TMAC unit is disclosed in Kalkunte, figure 6, element 22. **Claim 9 further specifies the switch further comprising an RMAC, which is missing from Kalkunte**. While this is not specifically disclosed in Yoshida, a switch that receives packets is disclosed in figure 7. It would have been obvious to one skilled in the art at the time of the invention to include a RMAC in the switch. **The motivation would be to have a unit to process the receiving of packets. Claim 9 also specifies 2 counters**. One is disclosed in figure 6, element 604 of Kalkunte. The

second is missing from Kalkunte. While it is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines 61-64. It would have been obvious to one skilled in the art at the time of the invention to have a second counter. **The motivation would be to be able to count the receive times.** Lastly, **claim 9 specifies QLN's that hold information corresponding to each packet, which is missing from Kalkunte**. However, Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. **The motivation would be to have all the information for each packet.** (*emphasis added*)

Applicants respectfully traverse the rejection.

Consistent with the above discussions of the patentability of claim 1, it is respectfully submitted that the features of recording the inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet into the (N+1)-th queue link node QLN(N+1) when the (N+1)-th packet is received by the switch, as specified in the recitation of the receiving process in claim 9, is not disclosed, taught, or suggested in the cited combination.

In addition, where the inter-packet gap IPG(M-1, M) between the (M-1)-th packet and the M-th packet is recorded in the M-th queue link node QLN(M) on the receiving of the M-th packet in the receiving process of claim 9, it is respectfully submitted that the features of: reading the M-th queue link node QLN(M) for obtaining the inter-packet gap IPG(M-1, M) when an M-th packet is transmitted by the switch; and utilizing the inter-packet gap IPG(M-1, M) as the basis of the inter-packet gap between the transmitted M-th and (M+1)-th packets, as recited for the transmitting process of claim 9, are not disclosed, taught, or suggested in the cited combination.

Therefore, Applicants respectfully submit that the cited combination by the Examiner fails to disclose, teach, or suggest all features recited in claim 9. For this reason, claim 9 is deemed clearly to be patentable over *Kalkunte* in view of *Yoshida*, and rejection of claim 9 should be withdrawn.

According to MPEP §2145, "A. Impermissible Hindsight",

> "[a]ny judgement on obviousness is in a sense necessarily a reconstruction based on hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper." *In re McLaughlin* 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971).

Applicants respectfully submit that the argument against the patentability of claim 9 presented in the Office Acton is based on impermissible hindsight reasoning. In particular, it is submitted that at least the following reason presented by the Examiner impermissibly relies on hindsight. The Examiner alleges that:

> **Claim 9 also specifies 2 counters**. One is disclosed in figure 6, element 604 of Kalkunte. The second is missing from Kalkunte. While it is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines 61-64. It would have been obvious to one skilled in the art at the time of the invention to have a second counter. **The motivation would be to be able to count the receive times**. (*emphasis added*)

However, Applicants' claim 9, as amended, recites:

> a **transmitting process**, the transmitting process comprising the steps of:
>
> (a1) proceeding to step (b1) when an M-th packet in the switch waits to be transmitted;
>
> (b1) reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M), and then transmitting the M-th packet;
>
> (c1) triggering the **second counter**;
>
> (d1) performing a counting operation by the **second counter**;
>
> (e1) proceeding to step (f1) when a counted value by the **second counter** is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), otherwise repeating said step (d1);

(f1) proceeding to step (g1) when an (M+1)-th packet in the switch waits for being transmitted, otherwise repeating said step (f1);

(g1) stopping the counting operation of the **second counter** and reading an (M+1)-th queue link node QLN(M+1) corresponding to an (M+1)-th packet for obtaining an inter-packet gap IPG(M, M+1), and then transmitting the (M+1)-th packet; and

(h1) increasing M by one and then repeating from said step (c1) to said step (h1). (*emphasis added*)

In the transmitting process, the second counter is used to count a counted value and a determination is made as to whether the counted value is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), which is the inter-packet gap between the receiving of the (M-1)-th and M-th packets in the receiving process. Thus, the second counter is **NOT** for counting the receive times. In view of the absence of any teaching or suggestion of this in the disclosures of *Kalkunte* and *Yoshida*, whether taken alone or in combination, as admitted by the Examiner, it is respectfully asserted that the Examiner has attempted to provide reasoning of motivation with respect to the second counter, only with knowledge from the Applicants' disclosure. It is respectfully submitted that the motivation asserted by the Examiner with respect to the second counter is improper, and this reasoning indicates that the judgement on obviousness of claim 9 is difficult without including knowledge gleaned only from Applicants' disclosure. For at least these reasons, it is respectfully submitted that the rejection of claim 9 is based upon impermissible hindsight reasoning, and the rejection accordingly should be withdrawn.

Furthermore, it is found that the Examiner *separately* considers only a selected portion of features of claim 9 and provides insufficient evidence that would fulfil the legal standard as recited in MPEP §2143 and explain how these separated features could be combined to meet all features of claim 9. Accordingly, Applicants respectfully submit that

the Examiner has failed to consider claim 9 ***as a whole*** and has pointed to ***no teaching within the prior art references that relates to the desirability of combining the selected features***. For this reason as well, it is submitted that the rejection of claim 9, as well as claim 10-14 depending from claim 9, is improper, and should be withdrawn.

Accordingly, it is respectfully submitted that claims 10-14 should be allowed for at least the reason that they depend from independent claim 9 with additional features therein, and the rejection of the claims should be withdrawn.

With respect to Applicants' independent claim 16, the Examiner alleges:

> Regarding claim 16, **one counter** is disclosed in figure 6, element 604 of Kalkunte. The second is missing from Kalkunte. While it is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines 61-64. It would have been obvious to one skilled in the art at the time of the invention to have a **second counter**. The motivation would be to be able to count the receive times.
>
> A **TMAC unit** is disclosed in Kalkunte, figure 6, element 22. Claim 16 further specifies the switch further comprising an **RMAC**, which is missing from Kalkunte. While this is not specifically disclosed in Yoshida, a switch that receives packets is disclosed in figure 7. It would have been obvious to one skilled in the art at the time of the invention to **include a RMAC in the switch**. The motivation would be to have a unit to process the receiving of packets."
>
> "Claim 16 also specifies **QLN's that hold information corresponding to each packet**, which is missing from Kalkunte. However, Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.
>
> The **TMAC** being used for reading the M-th QLN to obtain an IPG and then transmitting the M-th packet, then triggering the second counter, wherein when a counted value by the second counter is equal to a clock cycle value corresponding to the IPG, reading the next packet's IPG and transmitting next packet is disclosed in Kalkunte, in figure 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch)."

> Lastly, claim 16 specifies that the **RMAC is used for triggering the first counter to obtain an IPG between the N-th packet and the (N+1)-th packet, then recording the IPG**, which is missing from Kalkunte. This is disclosed in column 6, lines 61-64 of Yoshida. It would have been obvious to one skilled in the art at the time of the invention to use the receive process of Yoshida in conjunction with the transmit process of Kalkunte. The motivation would be to obtain an optimum transmission time for each packet. (*emphasis added*)

Applicants respectfully traverse the rejection.

Applicants' independent claim 16, as amended, recites:

> 16. An apparatus for transceiving a plurality of packets, wherein each of the packets corresponds to a queue link node, an N-th packet corresponds to an N-th queue link node QLN(N), and an M-th packet corresponds to an M-th queue link node QLN(M), where N and M are integrals, the apparatus comprising:
>
> a first counter and a **second counter**;
>
> a receive media access control (RMAC) unit for receiving the packets, wherein the RMAC unit is used for **triggering the first counter to obtain an inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet, and then recording the inter-packet gap IPG(N, N+1) into an (N+1)-th queue link node QLN(N+1)**; and
>
> a transmit media access control (TMAC) unit for transmitting the packets, wherein the TMAC unit is used for **reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M)**, and **then transmitting the M-th packet, and then triggering the second counter**, wherein **when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), an (M+1)-th queue link node QLN(M+1) corresponding to an (M+1)-th packet is read for obtaining an inter-packet gap IPG(M, M+1), and then the (M+1)-th packet is transmitted**.

It is respectfully submitted that the Examiner *separately* considers a selected portion of features of claim 16 and *separately* asserts the existence of motivation to combine with respect to the selected features. For some selected features of claim 16, such as the **second counter**, **RMAC**, and **QLN's that hold information corresponding to each packet**, even though there is no corresponding teaching, suggestion, or motivation found in *Kalkunte* or *Yoshida*, the Examiner *separately* provides alleged motivations of

usage of these features. However, referring to the previous discussions regarding the patentability of claims 1 and 9, from the Examiner's reasoning with respect to **QLN's that hold information corresponding to each packet, it CANNOT** be derived that the features related to queue link nodes corresponding to packets and inter-packet gaps are taught, disclosed, or suggested in the cited combination by the Examiner. For at least this reason, it is submitted that the cited combination fails to teach, disclose, or suggest all features recited in claim 16. Applicants therefore submitts that claim 16 clearly is patentable over *Kalkunte* in view of *Yoshida*, and the rejection of claim 16 should be withdrawn.

Moreover, it is respectfully submitted that the Examiner *separately* considers the selected features of claim 16 and provides no sufficient evidence that would fulfil the legal standard as recited in MPEP §2143 and explain how these separated features could be combined to meet all features of claim 16. Accordingly, Applicants respectfully submit that the Examiner has failed to consider claim 16 ***as a whole***, and has pointed to ***no teaching within the prior art references that relates to the desirability of combining the selected features***. For these reasons as well, it is submitted that the rejection of claim 16 is improper, and should be withdrawn.

Further, consistent with the discussions about patentability of claim 9, the **Office Action's ???** assertion motivation with respect to the second counter is improper, since the second counter is **NOT** for counting the receive times. In contrast, the second counter is used in together with the TMAC in order to transmit the M-th and (M+1)-th packets, according to the following recitation of claim 16:

a transmit media access control (TMAC) unit for transmitting the packets, wherein the TMAC unit is used for **reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M)**, and **then transmitting the M-th packet, and then triggering the second counter**, wherein **when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), an (M+1)-th queue link node QLN(M+1) corresponding to an (M+1)-th packet is read for obtaining an inter-packet gap IPG(M, M+1), and then the (M+1)-th packet is transmitted**.

In view of no teaching, suggestion, or motivation given in the disclosure of *Kalkunte* and *Yoshida*, as admitted by the Examiner, it is respectfully asserted that the Examiner has attempted to provide reasoning with respect to the second counter, that can be derived only with knowledge from the Applicants' disclosure. It is submitted that the motivation suggested by the Examiner with respect to the second counter is improper, and this reasoning indicates that the judgement on obviousness of claim 16 is difficult without including knowledge gleaned from Applicants' disclosure. For at least these reasons, it is respectfully submitted the rejection of claim 16 is based upon impermissible hindsight reasoning, and for this reason as well the rejection should be withdrawn.

Moreover, it is respectfully submitted that claims 17-22 are patentable for at least the reason that they depend from independent claim 16 with additional features therein, and the rejection of these claims also should be withdrawn.

Claims 8 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Kalkunte* in view of *Yoshida* in further view of Sanderson. Claims 8 and 15 are patentable over the cited combination for at least the reasons advanced above as to the patentability of independent claims 1 and 9 respectively, from which these claims respective depend, as well as for the additional features recited therein. Thus, withdrawal of the rejection is respectfully requested.

Conclusion

For the foregoing reasons, it is respectfully submitted that the application is in condition for allowance, and such a Notice with allowed claims 1-22, earnestly is solicited.

Should the Examiner feel that a conference would be helpful in expediting the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

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Date

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